General info(cover page) :

Lab 1: Digital logic gates

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Objectives: Understand the behavior and logic interpretation of different types of logic gates and practice the basis of circuit wiring and troubleshooting. Logic gates that will be evaluated are : NOT OR NOR AND NAND XOR, six gates in total.

Design:

We first set up the DC power supply and multi-meter, check if both are turned off, then switch multi-meter to measure for DC. Connect red lead to red multi-meter voltage input. For safety, the voltage input is set to be the range from 0V to 5V. After setting the DC power supply voltage output to zero, connect red lead of power supply to red lead of multi-meter. After turn on both multimeter and power supply, adjust till multimeter reads 5V, and turn it off.

First, I tested 74ALS04 gate. Insert chip onto breadboard. Identify VCC and GND, and connect VCC to red lead of power supply, GND to black lead of power supply. Choose one of the gate output connect to the red lead of multimeter, and black lead of multimeter to black lead of power supply at the GND pin. Next I connect a wire from VCC or GND to the input alternatively but not at the same time to observe different gate output and complete the truth table. This is the steps to complete observation of one logic gate and repeat those steps to five other gates to finish the lab. When completing the truth table, voltage around 4V is recognized as high, and below 1V is low. Gates are: NAND, NOR, AND, OR, XOR, NOT, six gates in total.

Results:

Below are the truth tables for six logic gates:

Table 1: Truth Table for Inverter (NOT Gate)

|  |  |  |
| --- | --- | --- |
| A(High/Low) | Y(Volts) | Y(High/Low) |
| Low | 4.39V | High |
| High | 0.109V | Low |

For NOT gate, high voltage input should result in low output, and vice versa.

Table 2:Truth Table for AND & OR Gates

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A(H/L) | B(H/L) | AND2(V) | AND2(H/L) | OR2(V) | OR2(H/L) |
| L | L | 110.6mV | L | 60mV | L |
| L | H | 110.8mV | L | 3.98V | H |
| H | L | 110.9mV | L | 3.98V | H |
| H | H | 4.418V | H | 3.98V | H |

For AND gate, only both high voltage inputs will result in high output. Else is all low output.

For OR gate, only both low input will result in low result. Else is all high output.

Table3: Truth Table for for NAND,NOR, & XOR Gates

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A(H/L) | B(H/L) | NAND2(V) | NAND(H/L) | NOR2(V) | NOR(H/L) | XOR2(V) | XOR(H/L) |
| L | L | 3.9V | H | 4.0V | H | 0.15V | L |
| L | H | 3.9V | H | 67mV | L | 4.4V | H |
| H | L | 3.98V | H | 67mV | L | 4.4V | H |
| H | H | 59mV | L | 66mV | L | 8.2mv | L |

For NAND gate, only both high input results in low output, else is all high.

Fir NOR gate, only both low input gives high output, else is all low.

For XOR gate, when two outputs are the same, output will be low, vise versa.

According to the tables above, it’s easy to observe the behaviors of all six logic gates, and all results of the output match the behaviors of corresponding gate. Again, output around 4V is recognized as high and below 1V is low.

Conclusion:

By setting up the circuit for logic gates, inputting different inputs, I got familiar with the behaviors of six types of logic gates.

Questions:

All truth tables are provided with explanation at above.

Feedback:

After carefully review the Lab as a whole, I think our lab is pretty good so far, just keep the way it is.